AMENDMENT TO THE CLAIMS

Claims 1-21 (canceled).

22. (New) A method comprising:

allowing a processor to execute instructions for improving a timing margin in a first integrated circuit (IC) die under test, wherein the execution

(a) instructs the first IC die to set a relative phase of receive and reference clock signals at the first IC die, from a plurality of discrete, receive phase values,

(b) instructs the first IC die to set a relative phase of transmit and reference clock signals at the first IC die, from a plurality of discrete, transmit phase values,

(c) instructs the first IC die to drive a sequence of outgoing data symbols according to the transmit clock and receive a sequence of incoming data symbols according to the receive clock, at the relative phase settings of (a) and (b), and compares the outgoing symbols to the incoming symbols, and then

(d) repeats (a)-(c) for other combinations of said plurality of transmit and receive phase values, and then

(e) sets the relative phases, to values which are closest to yielding a balanced timing margin as determined from the results of the comparisons.

23. (New) The method of claim 22 wherein the plurality of discrete, transmit phase values are predetermined positive and negative clock bias numbers with respect to a zero clock bias.

24. (New) The method of claim 23 wherein the zero clock bias represents a delay, immediately following a predefined transition of the distributed clock signal, that is one of approximately 1/4 cycle and approximately 3/4 cycle of the distributed clock signal.

25. (New) The method of claim 23 further comprising:

allowing the processor to execute further instructions to repeat (a) - (c) for all other combinations of said plurality of transmit and receive phase values, prior to (e).

26. (New) An article of manufacture comprising:

a machine-readable medium having instructions stored therein which, when executed by a processor, control a timing margin in an electronic system having first and second integrated circuit (IC) dies coupled to each other, the first IC die to drive a transmission line signal with a sequence of outgoing data symbols according to a transmit clock signal which is synchronized to a distributed clock signal, the first IC die to sample a transmission line signal to obtain a sequence of incoming data symbols according to a receive clock signal which is synchronized to the distributed clock signal, wherein execution of the instructions

(a) sets a relative phase of the receive and the distributed clock signals, from a plurality of discrete, receive phase values,

(b) sets a relative phase of the transmit and the distributed clock signals, from a plurality of discrete, transmit phase values,

(c) instructs the first IC die to drive the sequence of outgoing data symbols and receive the sequence of incoming data symbols, at the relative phase settings of (a) and (b), compares the outgoing symbols to the incoming data symbols and records a result of the comparison, and then

(d) repeats (a)-(c) for other combinations of said plurality of discrete, transmit phase values and discrete, receive phase values, and then

(e) sets the relative phases, as in (a) and (b), to a pair of values, from said plurality of discrete, transmit and receive phase values, which are closest to yielding a balanced timing margin as determined from the results of the comparisons.

27. (New) The article of manufacture of claim 26 wherein the machine-readable medium includes further instructions which, when executed by the processor, store the results of the comparisons in an array of variables each to be assigned one of a pass value and a fail value, wherein a pass means that the sequences of incoming and outgoing symbols substantially match and a fail means that they do not, and wherein each variable refers to the result of a comparison for a different pair of said plurality of discrete, receive and transmit phase values.

28. (New) The article of manufacture of claim 27 wherein the machine-readable medium includes further instructions which, when executed by the processor,

determine the largest timing margin by computing an average of the highest and lowest passing, discrete, transmit phase values, and an average of the highest and lowest passing, discrete, receive phase values in the array.

29. (New) An electronic system comprising:

first and second integrated circuit (IC) dies coupled to each other via one or more data transmission lines, and a processor coupled to access the first and second IC dies,

the first IC die to drive a transmission line signal, in one of the transmission lines, with a sequence of outgoing data symbols according to a transmit clock signal, the first IC die to derive the transmit clock signal from a distributed clock signal, which is distributed to the first and second IC dies,

the first IC die to repeatedly sample a transmission line signal, from one of the transmission lines, to obtain a sequence of incoming data symbols according to a receive clock signal, the first IC die to derive the receive clock signal from the distributed clock signal,

wherein the first IC die is to adjust (1) a relative phase of the transmit and distributed clock signals and (2) a relative phase of the receive and distributed clock signals, according to values stored in the first IC die and determined by the processor executing a program that evaluates data transfers between the first and second IC dies to obtain the values as yielding largest average timing margin for the data transfers.

30. (New) The electronic system of claim 29 wherein the transmission line includes one or more parallel traces formed in a printed wiring board on which the first and second IC dies are installed.

31. (New) The electronic system of claim 29 further comprising a clock signal generator coupled to provide the first and second IC dies with the distributed clock signal via a pair of parallel traces formed in a printed wiring board and to which an external clock input of the first die is connected.

32. (New) The electronic system of claim 31 further comprising a termination circuit, wherein the clock signal generator is coupled to one end of the pair of traces and the termination circuit is coupled to another end of the pair of traces, and wherein the pair of traces is looped through the second IC die.

33. (New) The electronic system of claim 32 wherein the distributed clock signal is provided to the driver timing circuitry and to the receiver timing circuitry from upstream and downstream locations, respectively, on the pair of traces.

34. (New) The electronic system of claim 29 wherein the receive delay is one of approximately zero cycle and approximately 1/2 cycle of the distributed clock signal, and the transmit delay is one of approximately 1/4 cycle and approximately 3/4 cycle of the distributed clock signal.

35. (New) The electronic system of claim 29 wherein the first IC die includes a dynamic random access memory storage array and the second IC die includes a memory controller.

36. (New) The electronic system of claim 29 wherein the first IC die includes a memory repeater and the second IC die includes a memory controller.

37. (New) A method comprising:

allowing a processor to execute instructions for improving a timing margin in first and second integrated circuit (IC) dies, wherein the execution

(a) sets a relative phase of receive and distributed clock signals at the first IC die, from a plurality of discrete, first receive phase values,

(b) sets a relative phase of receive and distributed clock signals at the second IC die, from a plurality of discrete, second receive phase values,

(c) instructs the second IC die to receive a sequence of outgoing data symbols according to the receive clock and the first IC die to receive a sequence of incoming data symbols according to the receive clock, at the relative phase settings of (b) and (a), respectively, and compares the outgoing symbols to the incoming symbols, and then

(d) repeats (a)-(c) for other combinations of said plurality of first and second receive phase values, and then

(e) sets the relative phases, as in (a) and (b), to values which are closest to yielding a balanced timing margin as determined from the results of the comparisons.

38. (New) The method of claim 37 wherein the plurality of discrete, first and second receive phase values are predetermined positive and negative clock bias numbers with respect to a zero clock bias.

39. (New) The method of claim 38 wherein the zero clock bias represents a delay, immediately following a predefined transition of the distributed clock signal, that is one of approximately zero cycle and approximately 1/2 cycle of the distributed clock signal.

40. (New) A method comprising:

allowing a processor to execute instructions for improving a timing margin in first and second integrated circuit (IC) dies, wherein the execution

(a) sets a relative phase of transmit and distributed clock signals at the first IC die, from a plurality of discrete, first transmit phase values,

(b) sets a relative phase of transmit and distributed clock signals at the second IC die, from a plurality of discrete, second transmit phase values,

(c) instructs the first IC die to drive a sequence of outgoing data symbols according to the transmit clock and the second IC die to drive a sequence of incoming data symbols according to the transmit clock, at the relative phase settings of (a) and (b), respectively, and compares the outgoing symbols to the incoming symbols, and then

(d) repeats (a)-(c) for other combinations of said plurality of first and second transmit phase values, and then

(e) sets the relative phases, as in (a) and (b), to values which are closest to yielding a balanced timing margin as determined from the results of the comparisons.

41. (New) The method of claim 40 wherein the plurality of discrete, first and second transmit phase values are predetermined positive and negative clock bias numbers with respect to a zero clock bias.

42. (New) The method of claim 41 wherein the zero clock bias represents a delay, immediately following a predefined transition of the distributed clock signal, that is one of approximately 1/4 cycle and approximately 3/4 cycle of the distributed clock signal.